

FIG. 1
BACKGROUND ART

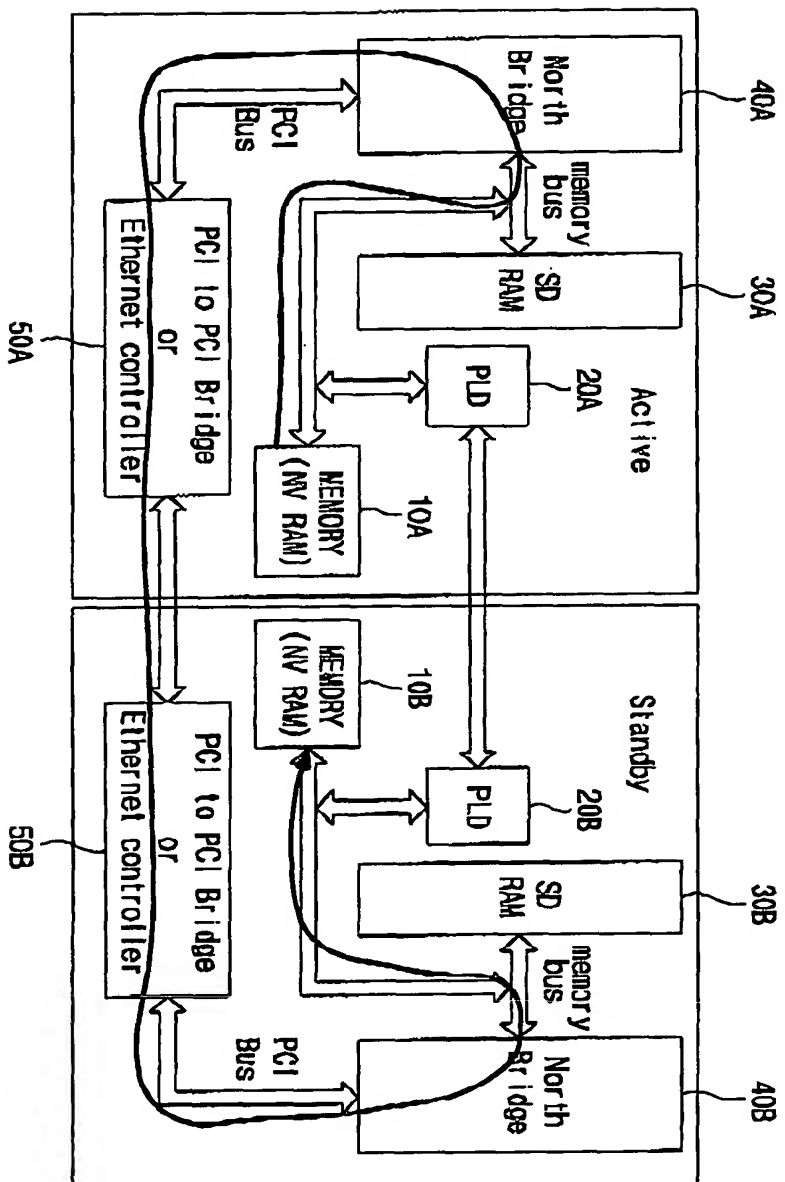


FIG. 2

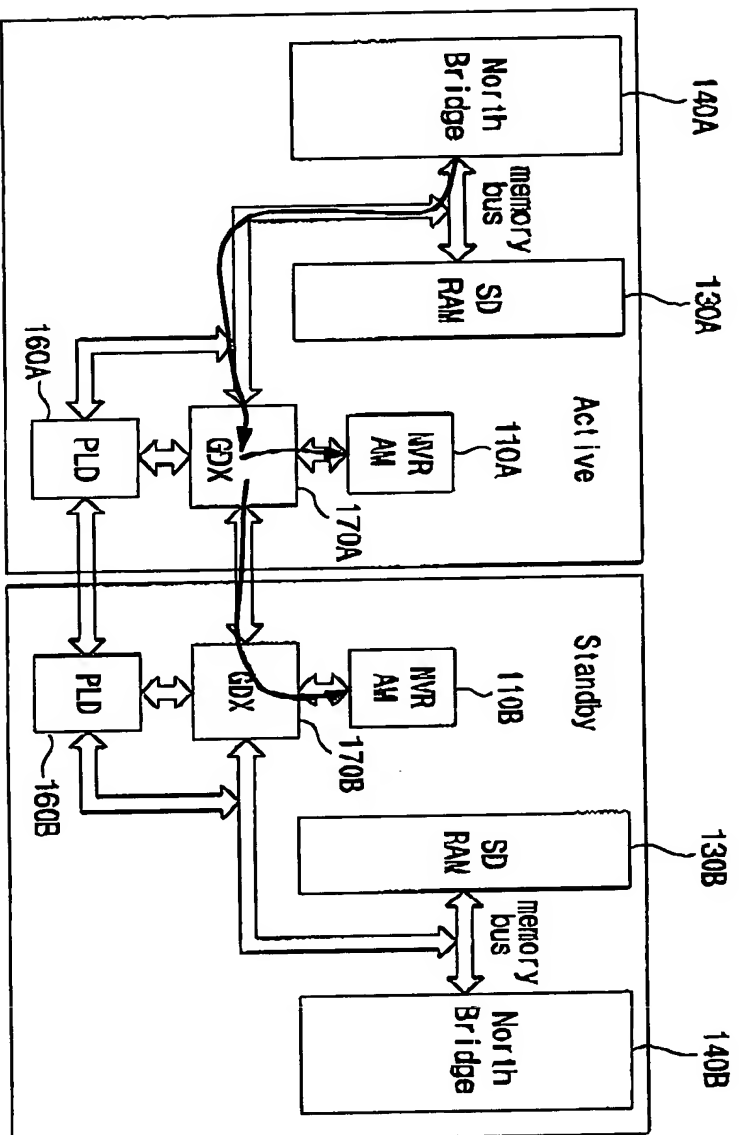


FIG. 3

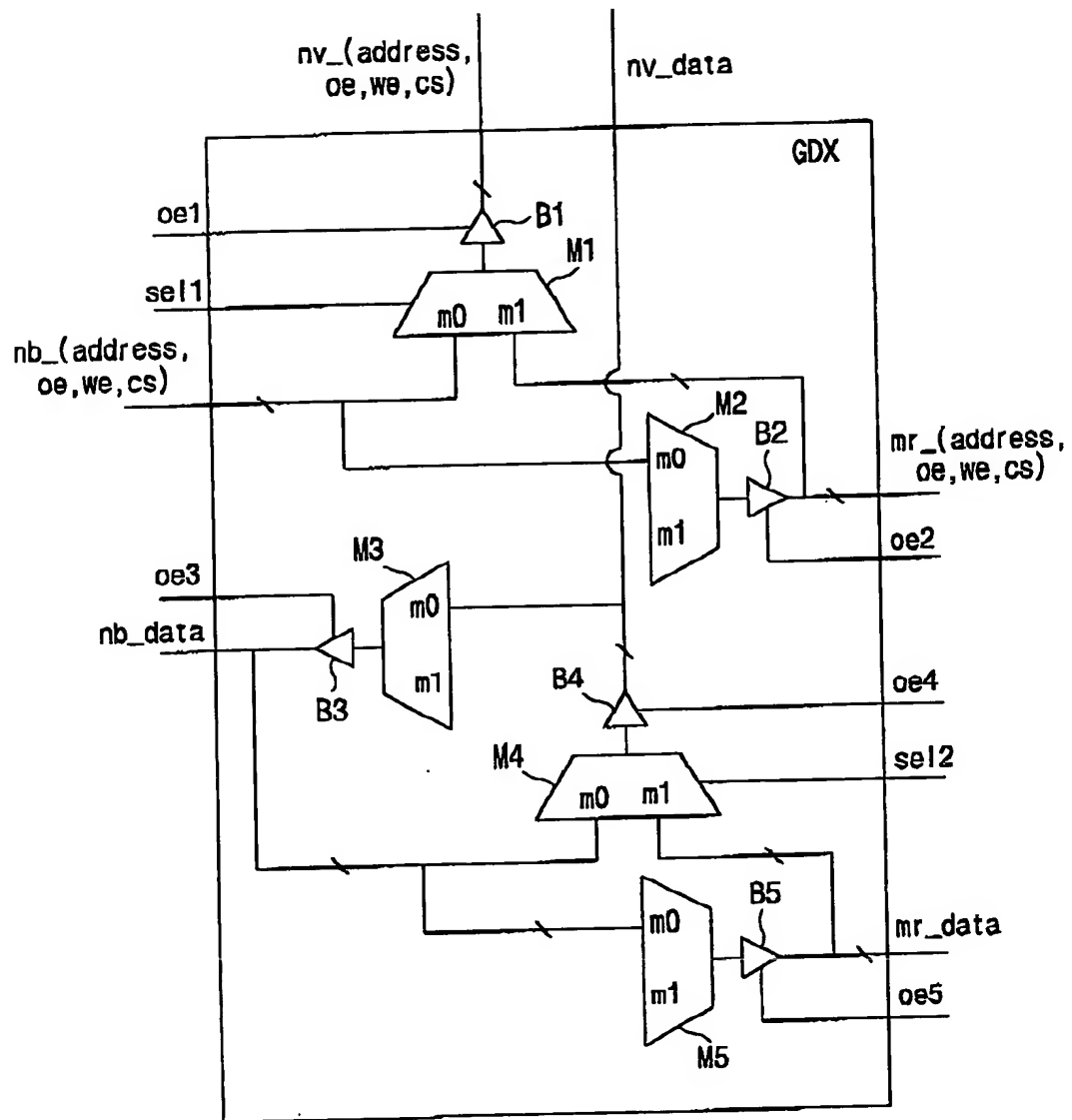


FIG. 4

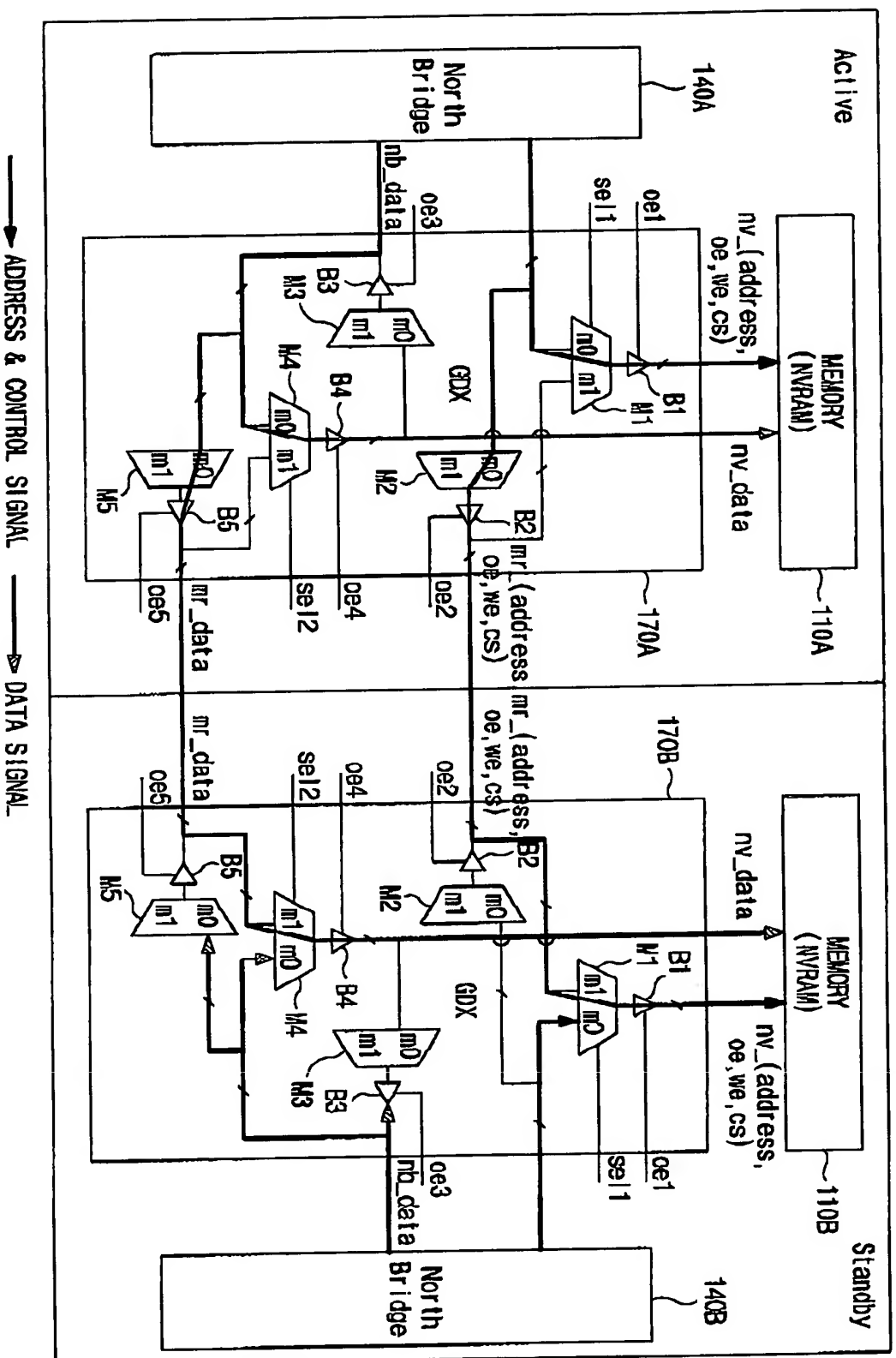


Figure 1 illustrates a dual-channel memory controller system, showing its operation in two states: Active and Standby.

Active State (Left):

- Channel 1 (Left):** Includes **MEMORY (NVRAM) 110A**, **nv_(address, oe, we, cs)** inputs, **nv_data** output, and **North Bridges 140A**. It features a multiplexer **B1** (m0/m1) controlled by **sel1**, a NAND gate **M1**, and a multiplexer **B2** (mr, oe, we, cs) controlled by **oe2**. A **GDIX** signal is also present.
- Channel 2 (Right):** Includes **MEMORY (NVRAM) 110B**, **nv_(address, oe, we, cs)** inputs, **nv_data** output, and **North Bridge 140B**. It features a multiplexer **B1** (m1/m0) controlled by **sel1**, a NAND gate **M1**, and a multiplexer **B2** (mr, oe, we, cs) controlled by **oe2**. A **GDIX** signal is also present.

Standby State (Right):

- Channel 1 (Left):** Includes **MEMORY (NVRAM) 110A**, **nv_(address, oe, we, cs)** inputs, **nv_data** output, and **North Bridges 140A**. It features a multiplexer **B1** (m0/m1) controlled by **sel1**, a NAND gate **M1**, and a multiplexer **B2** (mr, oe, we, cs) controlled by **oe2**. A **GDIX** signal is also present.
- Channel 2 (Right):** Includes **MEMORY (NVRAM) 110B**, **nv_(address, oe, we, cs)** inputs, **nv_data** output, and **North Bridge 140B**. It features a multiplexer **B1** (m1/m0) controlled by **sel1**, a NAND gate **M1**, and a multiplexer **B2** (mr, oe, we, cs) controlled by **oe2**. A **GDIX** signal is also present.

Legend:

- ADDRESS & CONTROL SIGNAL:** Indicated by a solid line with a triangle at the end.
- DATA SIGNAL:** Indicated by a solid line with a diamond at the end.

